WHAT IS CLAIMED IS:

1. A tape carrier package, comprising:

a chip having an active surface, wherein a plurality of bump electrodes are centrally arranged in two rows on the active surface;

a tape carrier, comprising:

a device hole having an area smaller than the chip; and

a plurality of leads, each of which being divided into inner lead and outer lead, wherein the inner leads are routed inward the center of the device hole and connected to the bump electrodes, respectively;

and

a sealing material encapsulating the active surface of the chip and the inner leads, with the outer leads being exposed.

2. The tape carrier package of claim 1, wherein a distance between the edge of the device hole and the adjacent bump electrodes in the direction of the inner leads are about 280 micron.

3. The tape carrier package of claim1, wherein the connection between the inner lead and the bump electrode is achieved by thermally pressing.

4. The tape carrier package of claim 1, wherein the bump electrodes are formed by bump formation process.

5. The tape carrier package of claim 1, wherein the chip is a rectangular chip, and the length of the device hole is substantially equal to that of the chip and the width of the device hole is smaller than that of the chip.

6. The tape carrier package of claim 1, further comprising:

two test bumps located at each end of the two rows of the bump electrodes; and

a test circuit around the edge of the chip on the active surface, wherein ends of the test circuit are electrically connected to the test bumps, respectively, and two of the leads are connected to the two test bumps, respectively.

7. The tape carrier package of claim 6, wherein the material of the test circuit includes polysilicon and metal.

8. The tape carrier package of claim 6, wherein the electric test of the chip is achieved by applying current to the test circuit to detect the defect at the edge of the circuit.

9. A chip suitable for detecting edge defects thereof by electrically testing, comprising:

an active surface;

a plurality of bump electrodes centrally arranged in two rows on the active surface;

two test bumps located at each end of the two rows of the bump electrodes; and

a test circuit around the edge of the chip on the active surface, wherein ends of the test circuit are electrically connected to the test bumps, respectively, and two of the leads are connected to the two test bumps, respectively.

10. The tape carrier package of claim 9, wherein the material of the test circuit includes polysilicon ad metal.

11. The tape carrier package of claim 1, further comprising a clearance between the active surface of the chip and the tape carrier, such that the sealing material flows out and cover the whole surface of the chip during sealing.

12. The tape carrier package of claim 11, wherein the clearance is about 10-60 micron.